

January 1996

ACS03MS

Radiation Hardened Quad 2-Input NAND Gate with Open Drain

Pinouts Features • Devices QML Qualified in Accordance with MIL-PRF-38535 **14 PIN CERAMIC DUAL-IN-LINE** MIL-STD-1835 DESIGNATOR CDIP2-T14. · Detailed Electrical and Screening Requirements are Contained in LEAD FINISH C SMD# 5962-96703 and Intersil's QM Plan TOP VIEW 1.25 Micron Radiation Hardened SOS CMOS 14 VCC A1 1 13 B4 B1 2 Single Event Upset (SEU) Immunity: <1 x 10⁻¹⁰ Errors/Bit/Day 12 A4 Y1 3 (Typ) 11 Y4 A2 4 B2 5 10 B3 Y2 6 9 A3 8 Y3 GND 7 • Latch-Up Free Under Any Conditions • Military Temperature Range-55°C to +125°C • Significant Power Reduction Compared to ALSTTL Logic DC Operating Voltage Range 4.5V to 5.5V **14 PIN CERAMIC FLATPACK** MIL-STD-1835 DESIGNATOR CDFP3-F14, Input Logic Levels LEAD FINISH C - VIL = 30% of VCC Max TOP VIEW - VIH = 70% of VCC Min 1. 14 77 Input Current ≤ 1µA at VOL, VOH 13 2 2**7** B4 77. • Fast Propagation Delay 15ns (Max), 10ns (Typ) 3 12 22 4 11 27 22 Description 5 77 10 The Intersil ACS03MS is a Radiation Hardened quad 2-input NAND gate 72 6 9 77 ___ A3 with open drain outputs. The open drain output can drive resistive loads 7 GND 🗖 27-8 ⊐ Y3 from a separate supply voltage. The ACS03MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic Family. The ACS03MS is supplied in a 14 lead Ceramic Flatpack (K suffix) or a

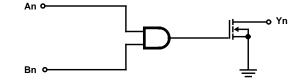
Ordering Information

Ceramic Dual-In-Line Package (D suffix).

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9670301VCC	-55°C to +125°C	MIL-PRF-38535 Class V	14 Lead SBDIP
5962F9670301VXC	-55°C to +125°C	MIL-PRF-38535 Class V	14 Lead Ceramic Flatpack
ACS03D/Sample	25°C	Sample	14 Lead SBDIP
ACS03K/Sample	25°C	Sample	14 Lead Ceramic Flatpack
ACS03HMSR	25°C	Die	Die

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures. http://www.intersil.com or 407-727-9207 | Copyright © Intersil Corporation 1999

Functional Diagram



TRUTH TABLE

INP	UTS	OUTPUT
An	Bn	Yn
L	L	Z (Note 2), H (Note 3)
L	Н	Z (Note 2), H (Note 3)
Н	L	Z (Note 2), H (Note 3)
Н	Н	L

NOTES:

1. L = Low, H = High, Z = High Impedance

2. Without Pull-up Resistor

3. With Pull-up Resistor

Die Characteristics

DIE DIMENSIONS:

68 mils x 79 mils 1730mm x 2010mm

METALLIZATION:

Type: AlSi Metal 1 Thickness: 7.125kÅ ±1.125kÅ Metal 2 Thickness: 9kÅ ±1kÅ

GLASSIVATION:

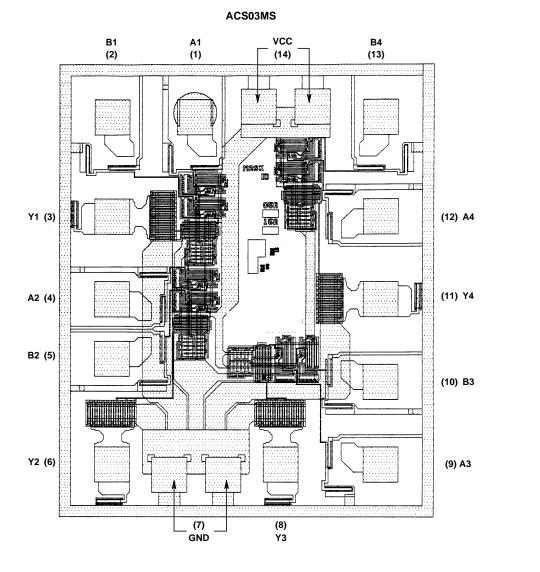
Type: SiO₂ Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY: <2.0 x 10⁵A/cm²

BOND PAD SIZE:

110μm x 110μm 4.3 mils x 4.3 mils

Metallization Mask Layout



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